In the Claims:

Please replace claim 16 all as shown below. All pending claims are reproduced below, including unchanged claims and marked up versions of amended claims.

13. (Original) A method for manufacturing a dual gate transistor device, comprising:
(a) providing a substrate having a buried oxide region;
(b) depositing a first nitride mask layer having a pattern overlying a silicon region;
(c) forming a trench in said substrate with a depth to said buried oxide;
(d) depositing a conformal oxide in said trench;
(e) forming vias in said conformal oxide adjacent to said silicon region and removing a portion of said first nitride mask to expose a portion of said silicon region;
(f) depositing polysilicon in said vias and on said portion of said silicon region; and
(g) implanting an impurity into exposed portions of polysilicon in said trench and of said silicon-on-insulator substrate underlying said second nitride layer.

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14. (Original) The method of claim 13 wherein said step (c) is performed by: depositing a nitride mask layer; forming a trench window in said nitride mask layer; and etching said substrate to expose said buried oxide.

15. (Original) The method of claim 13 wherein said step (d) is performed by: depositing a TEOS layer to fill the trench to a level equivalent to said first nitride mask layer.

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16. (Currently Amended) The method of claim 13 wherein said step (e) comprises:
depositing a photoresist~~gate~~ layer; and
etching the vias and the first nitride layer through an opening formed in said photoresist~~gate~~ layer.

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17. (Previously Amended) The method of claim 13 wherein said step (f) comprises: implanting arsenic at an energy of 15-20 KeV with a zero degree tilt to provide a concentration of 2-4x10^{15}/cm^3.

18. (Previously Amended) The method of claim 13 wherein said step (f) comprises: depositing phosphorous at an energy of 7-10 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-4x10^{15}/cm^3.

19. (Previously Amended) The method of claim 13 wherein said step (f) comprises: depositing boron at an energy of 1.5-2.5 KeV with a zero degree tilt to provide a concentration of the impurity in a range of 2-3x10^{15}/cm^3.

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20. (Original) The method of claim 13 further including the step, between steps (f) and (g),

of:

polishing the polysilicon and substrate.

21. (Original) The method of claim 13 further including the step, between said steps (e) and (f), of:

growing a gate oxide about the silicon region in said vias.

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